Laboratory for Computer Architecture

Energy-Aware Application Scheduling on a Heterogeneous Multi-core System

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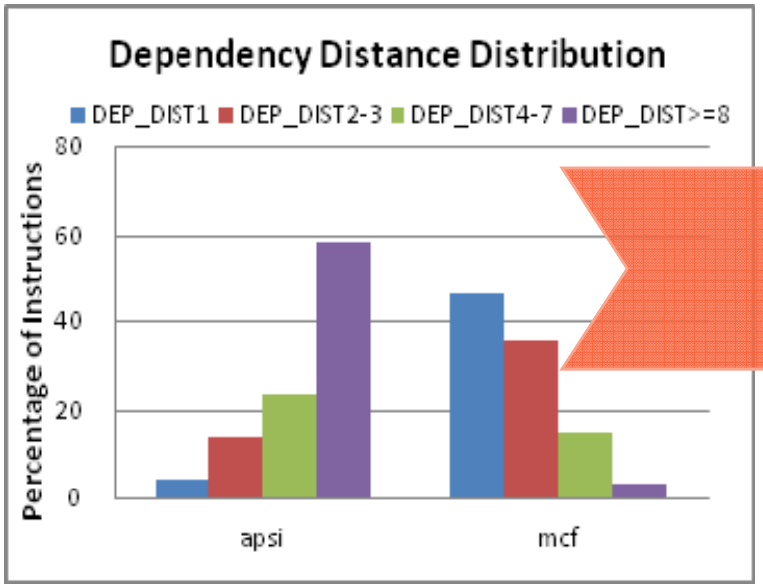
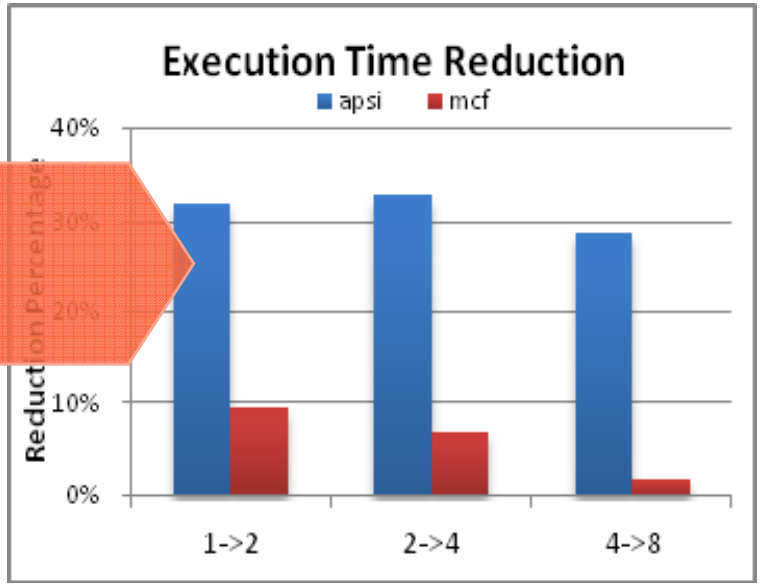
Introduction & Motivation

- **Heterogeneous multi-core processor**
  - Static : Cell [Hofstee, HPCA'05]
  - Dynamic : Core Fusion [Ipek ISCA'07], Tflex[Kim Micro'07]
  - Meet diverse computational requirements.
- **Program scheduling**
  - Dynamic trial-and-error approach [Kumar, Micro'03]
    - Context switching overhead
    - Not scalable

Introduction & Motivation (Cont.)

- **Program's inherent characteristics**
  - Define the computational requirements
  - Can be leveraged to guide the program scheduling in heterogeneous computing environment.
- **Example:**



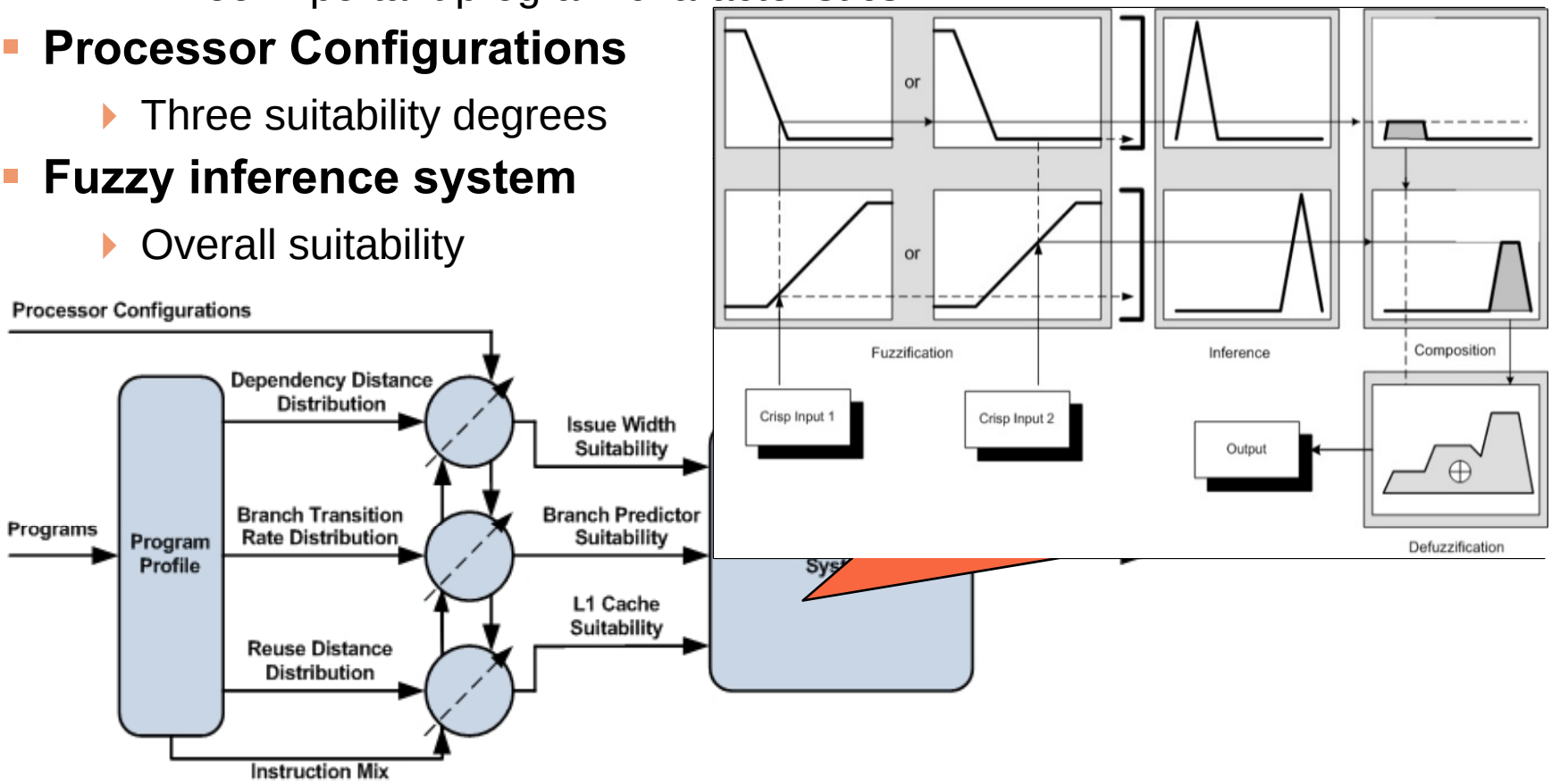


Outline

- **Overview of the Fuzzy Logic Approach**
- **Suitability Metrics**
  - Issue Width Suitability
  - Branch Predictor Suitability
  - Cache Suitability
- **Evaluation**
  - Experiment Setup
  - Experimental Results
- **Conclusion**

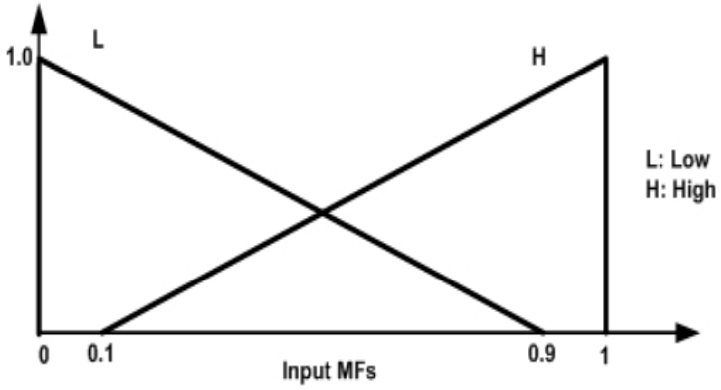
Overview of the Fuzzy Logic Approach

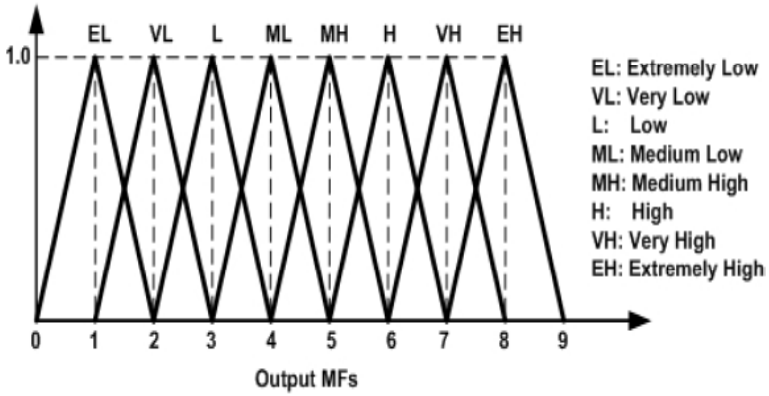
- **Program profile**
  - Three important program characteristics
- **Processor Configurations**
  - Three suitability degrees
- **Fuzzy inference system**
  - Overall suitability



Rule Set

IF			THEN
Issue Width Suitability	**Branch Predictor Suitability**	**Cache Size Suitability**	**Overall Suitability**
Low	Low	Low	EL
Low	Low	High	VL
Low	High	Low	L
High	Low	Low	ML
Low	High	High	MH
High	Low	High	H
High	High	Low	VH
High	High	High	EH





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Suitability Metrics – Issue Width Suitability

- **Measures the match between the program's ILP and the processor's issue width.**
  - The center of the mass (weighted average) of the dependency distance distribution
  - The distance between the mass center and the node represented by the issue width
- **Need to complement the corresponding condition of the rule**

$$IssueWidthSuitability(i) = \left| X_i - \frac{\sum_{i=1}^{4} P_i * X_i}{\sum_{i=1}^{4} P_i} \right|$$

X_i, i=1..4, are the x coordinates of the nodes representing the issue width. P_i i=1..4, are the percentage of instructions that can be best exploited with issue width X_i.

Suitability Metrics – Branch Predictor Suitability

- **Measure the match between program's branch predictability and the branch predictor size.**
  - Branch transition rate [Haungs, HPCA'00]
  - Buckets [0,0.1], [0.1,0.2], [0.2,0.3] … [0.9,1.0]
  - The center of the mass (weighted average) of the distribution
- **Need to complement the corresponding condition of the rule**

$$BranchFeatability(i) = \left| B_i - \frac{(B_1 \cdot (P_2 + P_0) + B_2 \cdot (P_1 + P_6) + B_3 \cdot (P_4 + P_7) + B_4 \cdot w \cdot \sum_{i=4}^{7} P_i)}{\sum_{i=4}^{4} P_i + \sum_{i=7}^{7} P_i + w \cdot \sum_{i=4}^{5} P_i} \right|$$

B_i, i=1..4, are the x coordinates of the nodes representing the sizes of the branch predictors, w is the weight.

Suitability Metrics – Cache Suitability

- **Measure the degree of the match between the program's data locality and the cache size.**
- **No similar relationship between the reuse distance and the corresponding desired L1 cache size.**
- **Cache Efficiency:**
  - Calculates how much program locality per unit cache size captures
  - Need to be normalized so that the value is in [0,1]

$$CacheSuitability = \frac{\left(\frac{P_{R<Ci}}{Ci}\right)}{\left(\frac{P_{R<Ci}}{Ci}\right)_{max}}$$

$P_{R<Ci}$, i=1..4, are the percentage of data accesses with reuse distance less than C_i. C_i i=1..4, are the L1 cache size of core i.

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Experiment Setup

- Single-ISA quad-core heterogeneous processor, with each core an out-of-order processor
- X_i and B_i, $i=1..4$, are set to 0.125, 0.25, 0.5, and 1.
- Simpoint Interval with 100Million Instructions for SPECcpu 2000 benchmarks
- Using Wattch to collect power and performance data.

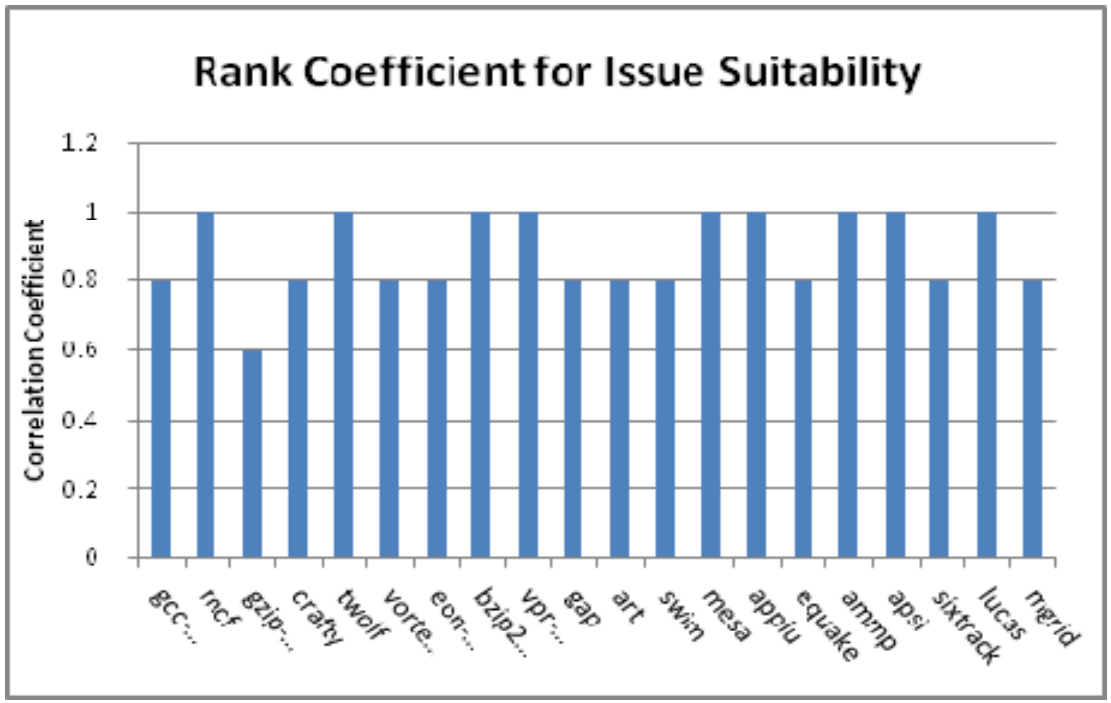
Items	Configuration Options
Issue Width	single-issue, 2-issue, 4-issue, 8-issue
L1 D-Cache	16KB, 4-way, block size 64byte, 32KB, 4-way, block size 64byte, 64KB, 4-way, block size 64byte, 128KB, 4-way, block size 64byte
Branch Predictor	1K Gshare, 2K Gshare, 4K Gshare, 8K Gshare

Items	Configurations
Core 1	Out-of-order, 2-issue, Gshare(1k), 16k 4-way L1 d-cache 64byte, 32k 2-way i-cache 64byte, 512k L2 cache
Core 2	Out-of-order, 2-issue, Gshare(1k), 32k 4-way L1 d-cache 64byte, 32k 2-way i-cache 64byte, 512k L2 cache
Core 3	Out-of-order, 4-issue, Ghsare(4k), 32k 4-way L1 d-cache 64byte, 32k 2-way i-cache 64byte, 512k L2 cache
Core 4	Out-of-order, 8-issue, Gshare(8k), 64k 4-way L1 d-cache 64byte, 32k 2-way i-cache 64byte, 512k L2 cache

Experimental Results (1)

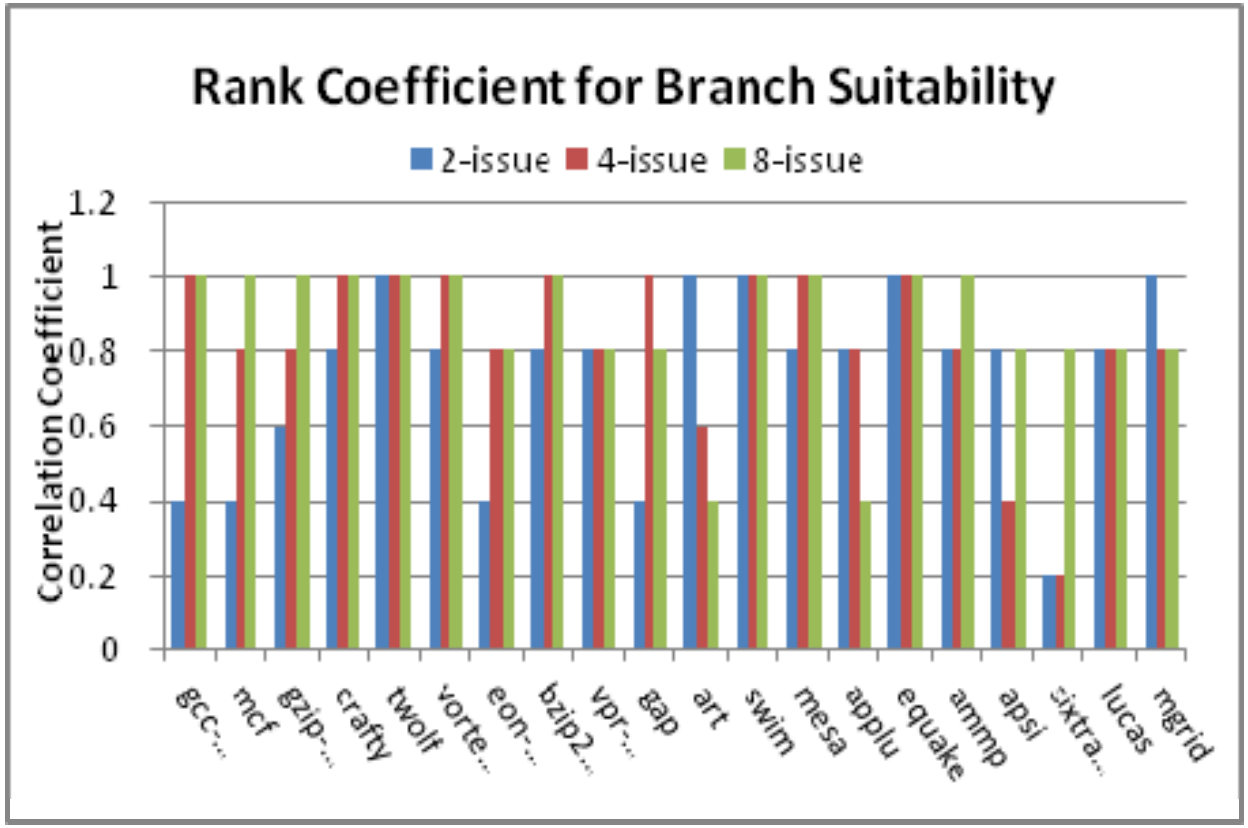
- Evaluation of issue width suitability
  - Spearman's Rank Coefficient:

$$\rho = 1 - \frac{6 \sum d_i^2}{n(n^2 - 1)}$$, d_i is the rank difference



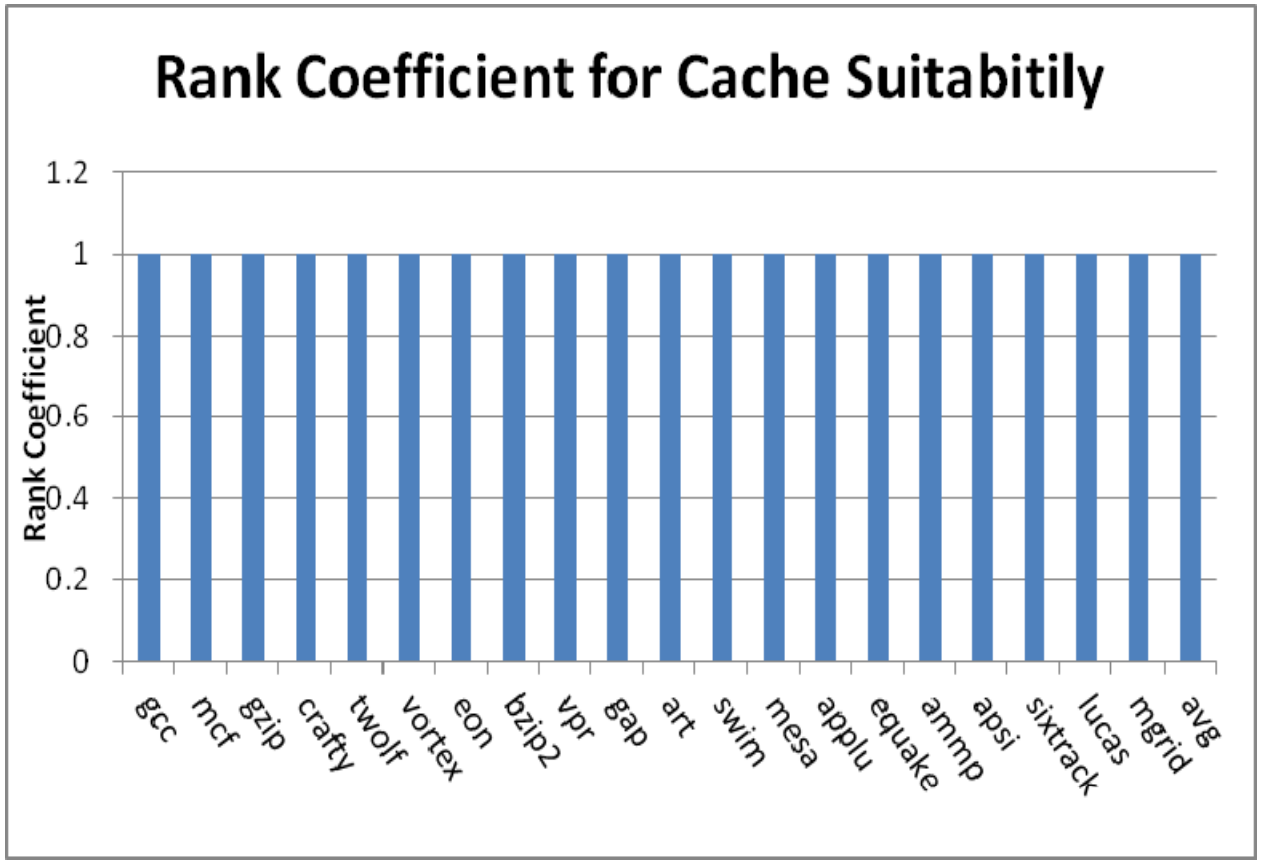
Experimental Results (2)

- Evaluation of branch predictor suitability



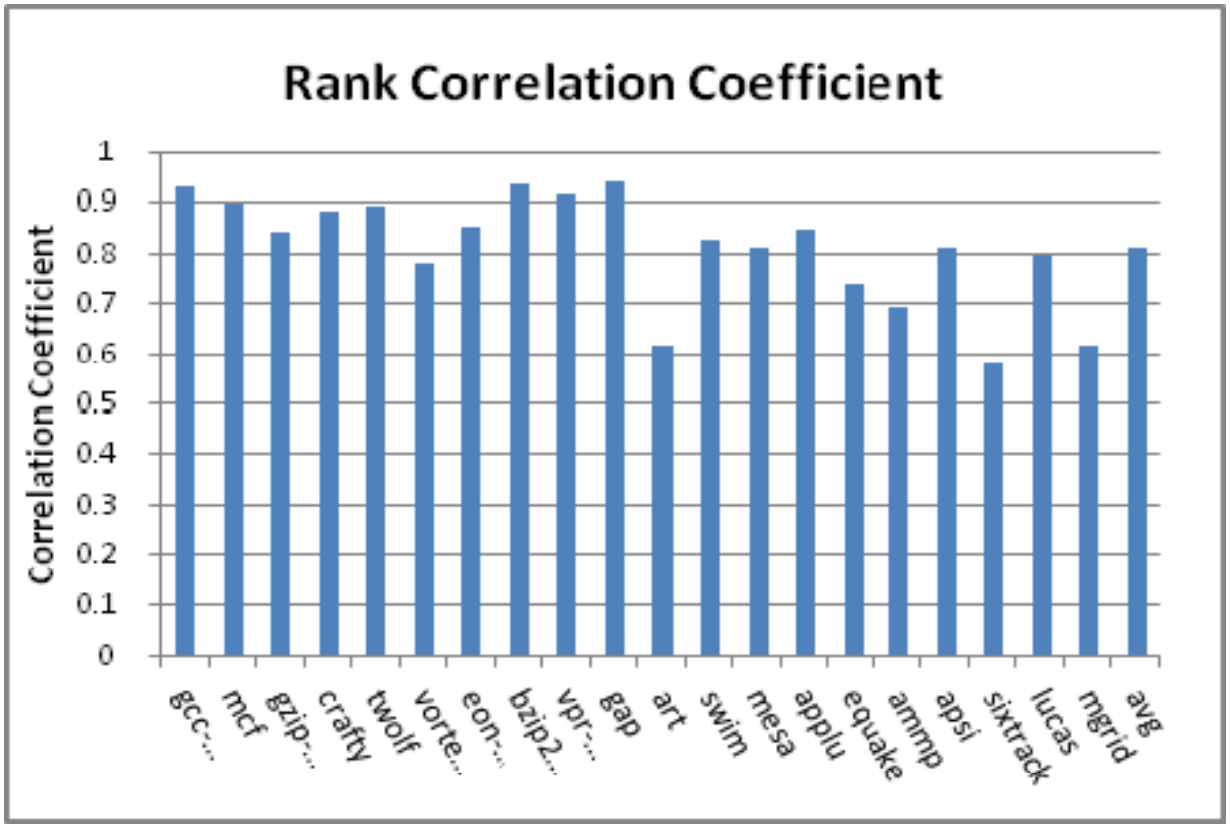
Experimental Results (3)

- Evaluation of cache suitability.



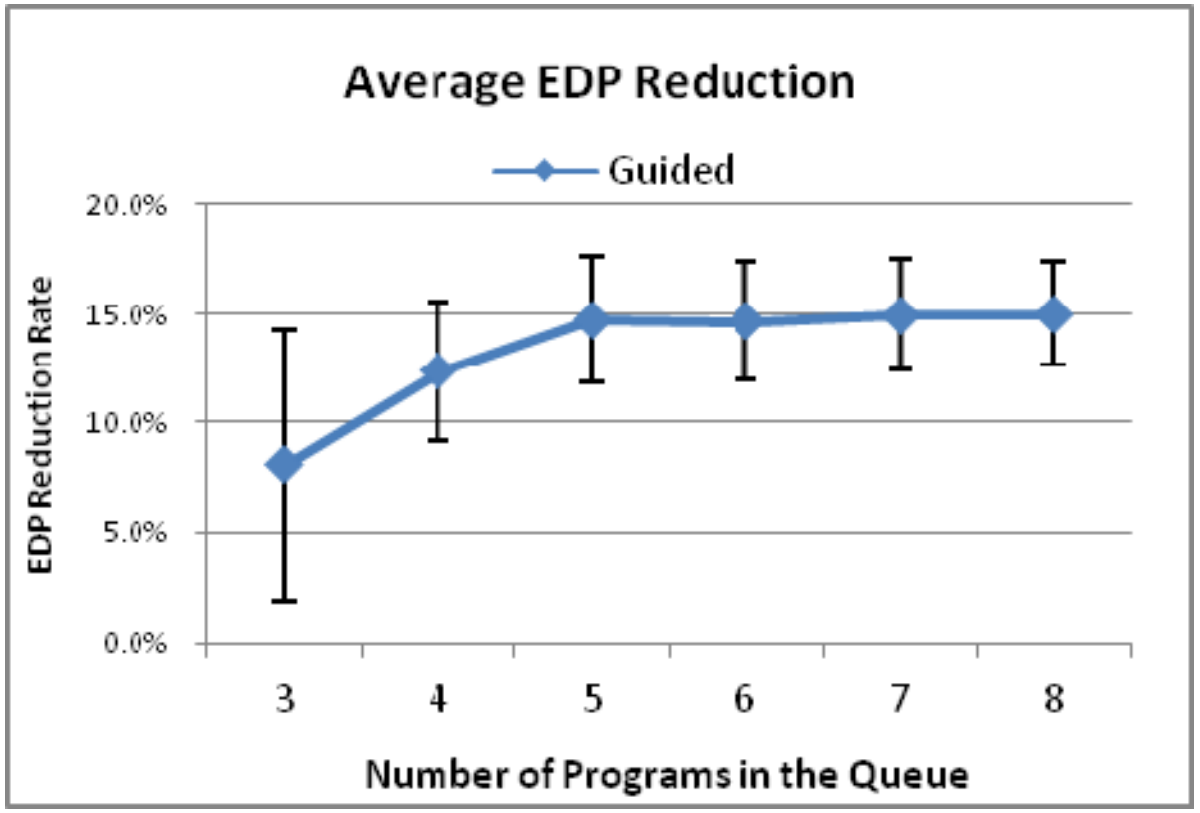
Experimental Results (4)

- Evaluation of overall suitability



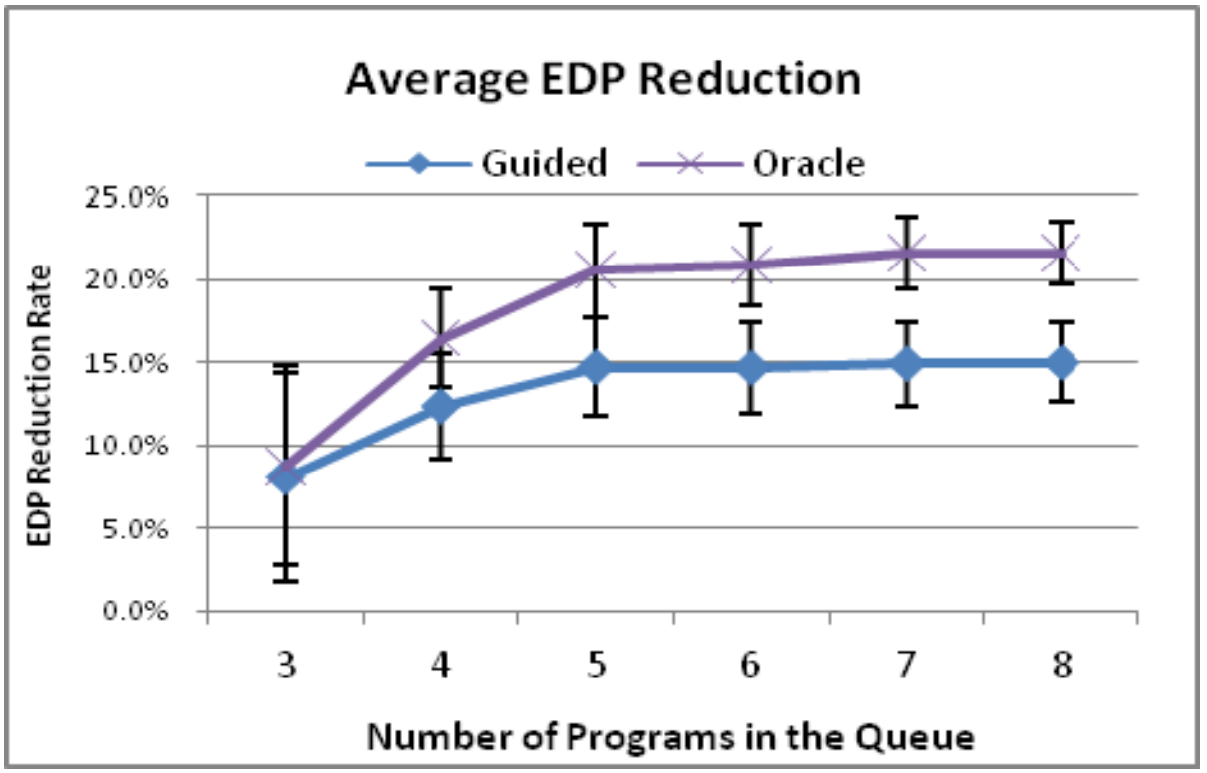
Experimental Results(5)

- **Average EDP reduction rate of the suitability-guided scheduling compared with the random scheduling.**



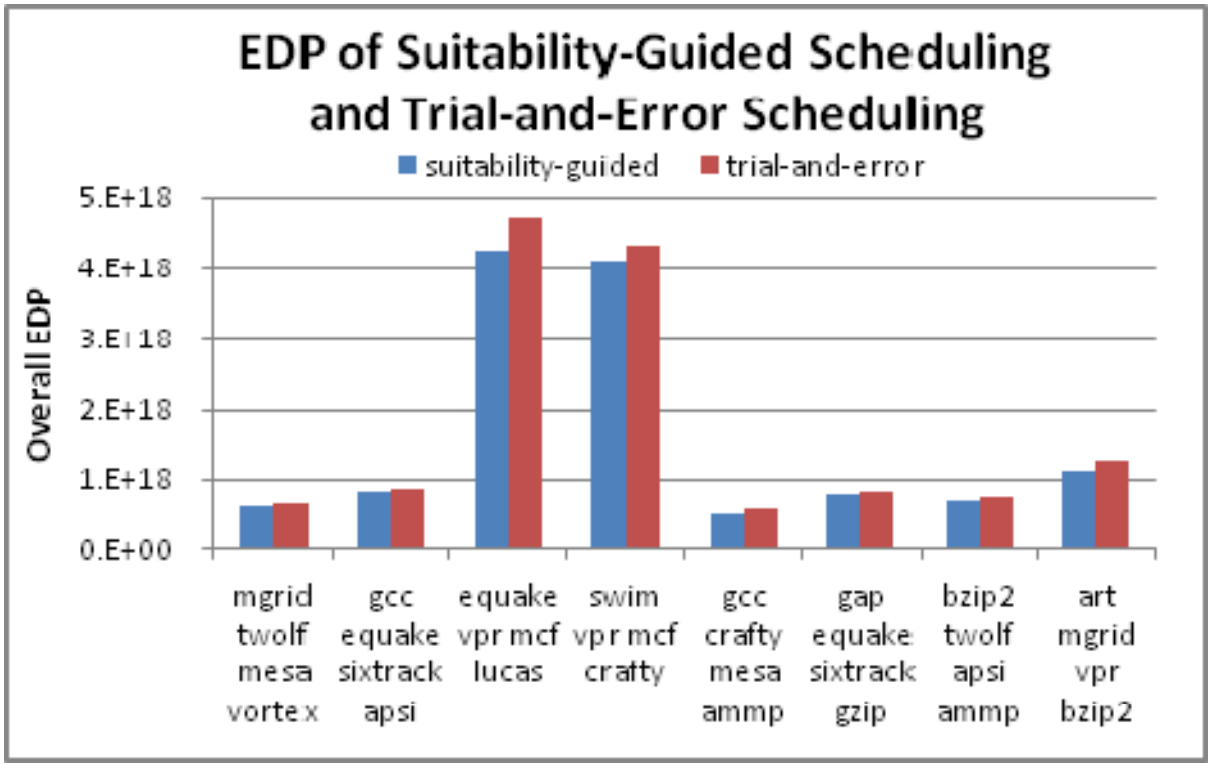
Experimental Results(6)

- EDP reduction rate comparison between the suitability guided scheduling and the oracle scheduling (random scheduling as the baseline)



Backup -- Experimental Results(5)

- EDP comparison between suitability-guided scheduling and Trial-and-error scheduling



Conclusion & Future work

- **A fuzzy logic based approach to schedule the program to its optimum core in heterogeneous multi-core.**
- **The method achieves 15% average reduction in EDP compared with that of the random scheduling approach**

- **Future Work**
  - More program characteristics in determining the suitability.
  - The effects of resource sharing and inter-core communication.
  - Extension to dynamic heterogeneous multi-core processor.

Thank You

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