Evaluating Performance of BLAST on Intel Xeon and Itanium2 Processors

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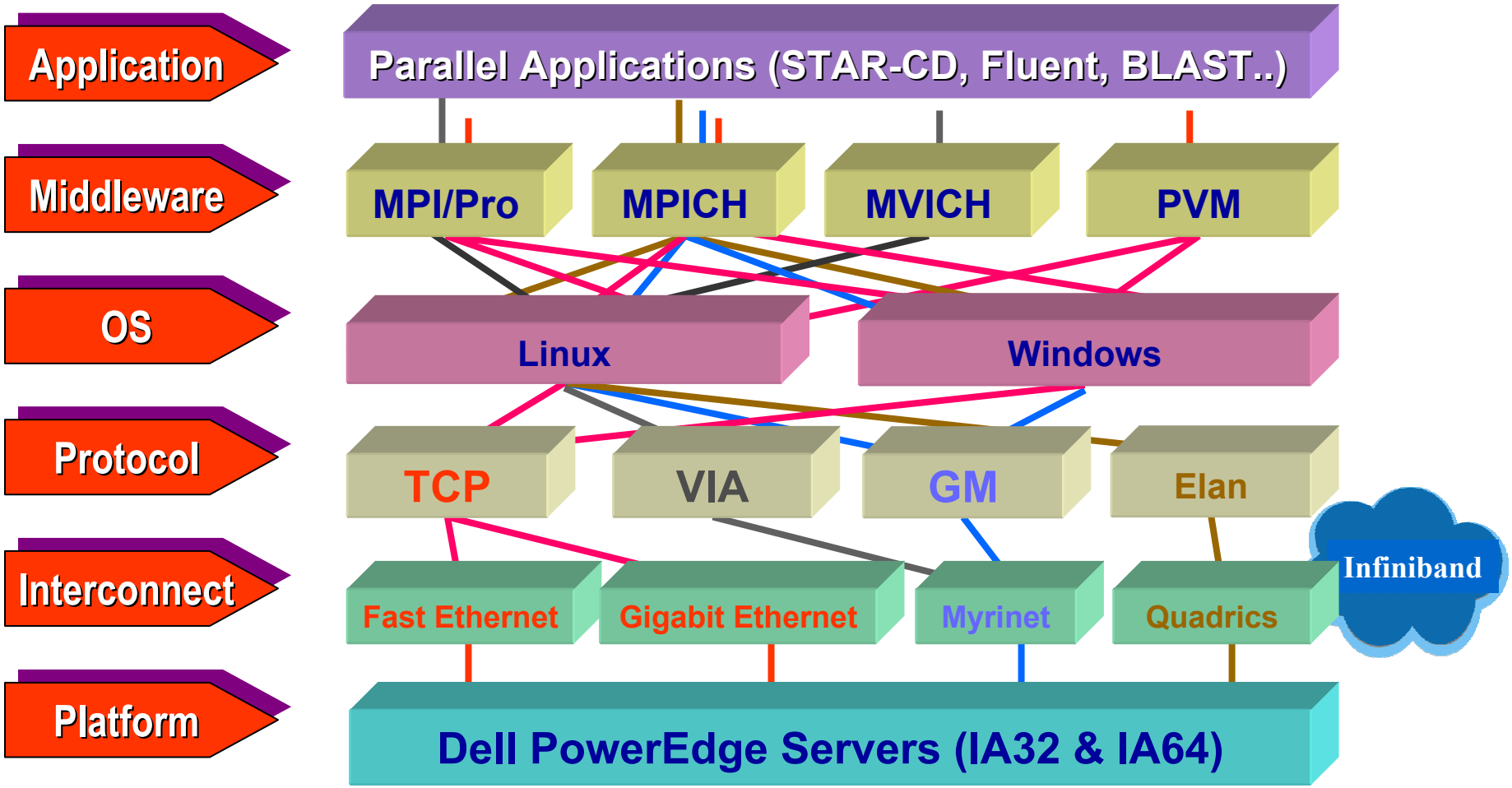
Agenda

- **Objectives**
- **Platform Comparison**
  - Xeon and Itanium2 Processors
  - Cache and Memory architecture
- **BLAST**
  - Application Characteristics
- **Experimental Setup**
- **Performance Analysis**
  - Memory System Performance
  - Application performance
  - Workload Characterization
- **Future Work**

HPCC Building Blocks



Objectives

- **Evaluate performance of BLAST on different Intel Processor Architectures**
  - **Nocona – 90nm Xeon**
  - **Prestonia – 130 nm Xeon**
  - **Madison – Itanium2**
- **Platform Comparison**
  - **Impact of Processor FSB and Memory differences**
- **BLAST**
  - **Application Performance**
  - **Application Characteristics**

- **Dell PowerEdge Servers**
  - **PE1750 (IA32)**
    - **Dual 3.2Ghz Processors, 533MHz FSB**
    - **L2 Cache: 512KB, L3: 1MB**
    - **DDR-266 MHz**
  - **PE1850 (EM64T)**
    - **Dual 3.2Ghz Processors, 800MHz FSB**
    - **Dual 3.6Ghz Processors, 800MHz FSB**
    - **L2 Cache: 1024KB**
    - **DDR2-400 MHz**
  - **PE3250 (IA64)**
    - **Dual 1.5Ghz Itanium2 Processors, 400MHz FSB**
    - **L2 Cache: 256KB, L3: 6MB**
    - **DDR-200 MHz**

- **Xeon DP (130nm) - Prestonia**
  - **1.8Ghz – 3.2Ghz, 400MHz – 533MHz (FSB)**
  - **20 stage pipeline**
- **Xeon DP (90nm) - Nocona**
  - **2.8Ghz – 3.6Ghz, 800 MHz (FSB)**
  - **31 stage pipeline**
  - **x86 64bit Extensions**
- **Itanium2 - Madison**
  - **1.0Ghz - 1.5Ghz, 400MHz FSB**
  - **64-bit EPIC architecture**

Cache and Memory subsystem Comparison

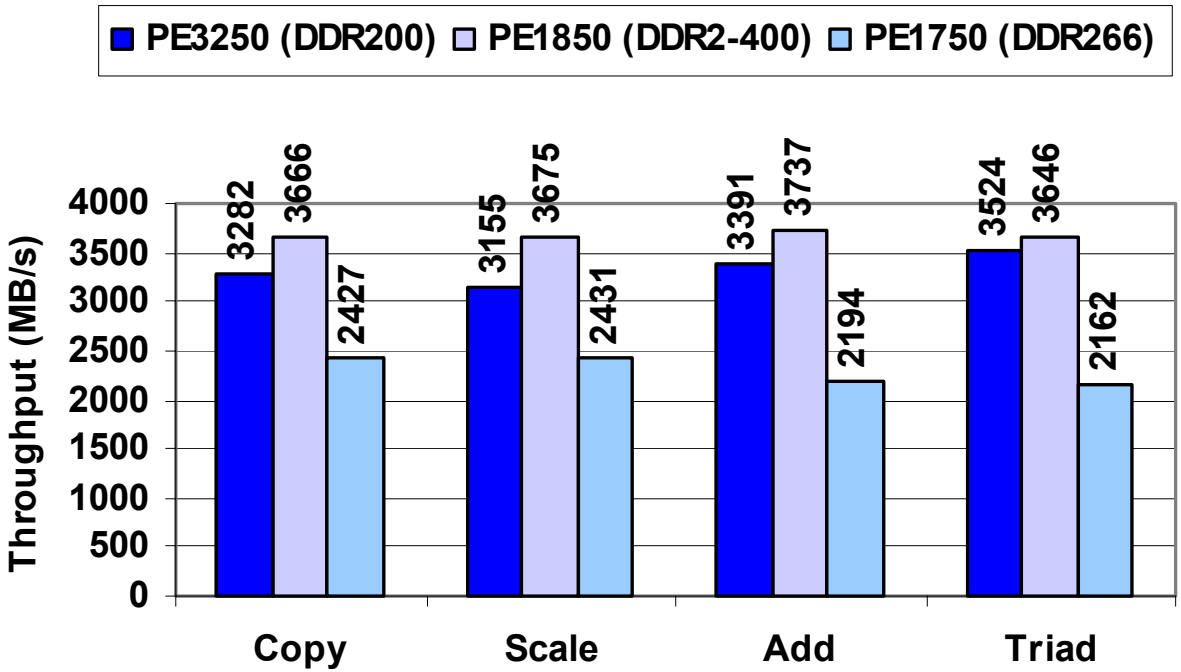
- **Memory Subsystem Differences:**
  - **DDR vs. DDR2**

- **Cache Architectures**

	PE1750 Xeon 130nm	PE1850 Xeon 90nm	PE3250 Itanium2
L1 (Inst Cache)	12K μops Trace Cache	12K μops Trace Cache	16KB
L1 (Data Cache)	8KB	16KB	16KB
L2 Cache	512KB	1024KB	256KB
L3 Cache	1MB	N/A	6MB

- **Theoretical Peak Bandwidth:**
  - **PE3250 – 6.4 GB/s**
  - **PE1850 – 6.4GB/s**
  - **PE1750 – 4.2GB/s**

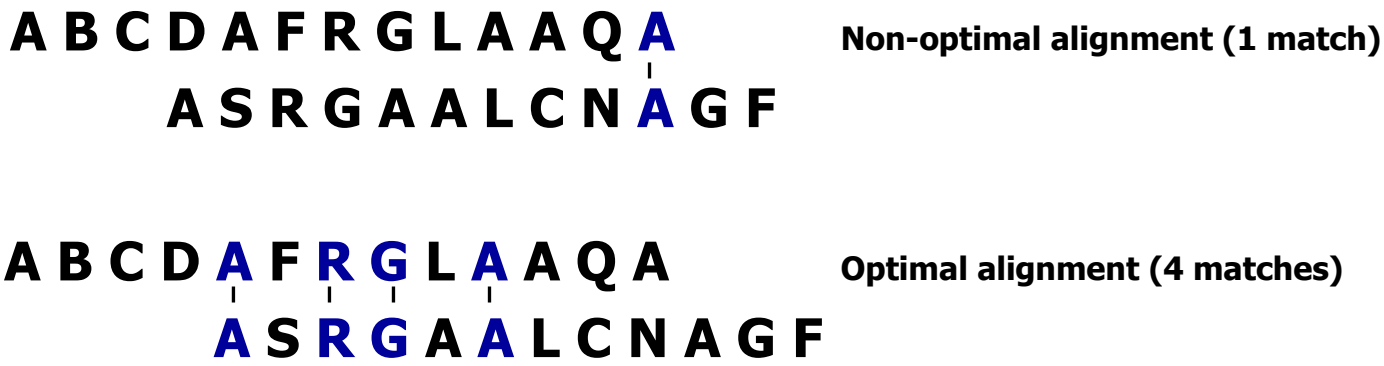
- **Sustainable memory bandwidth:**



- **Cache Access and Memory Read Latency (using LMbench)**

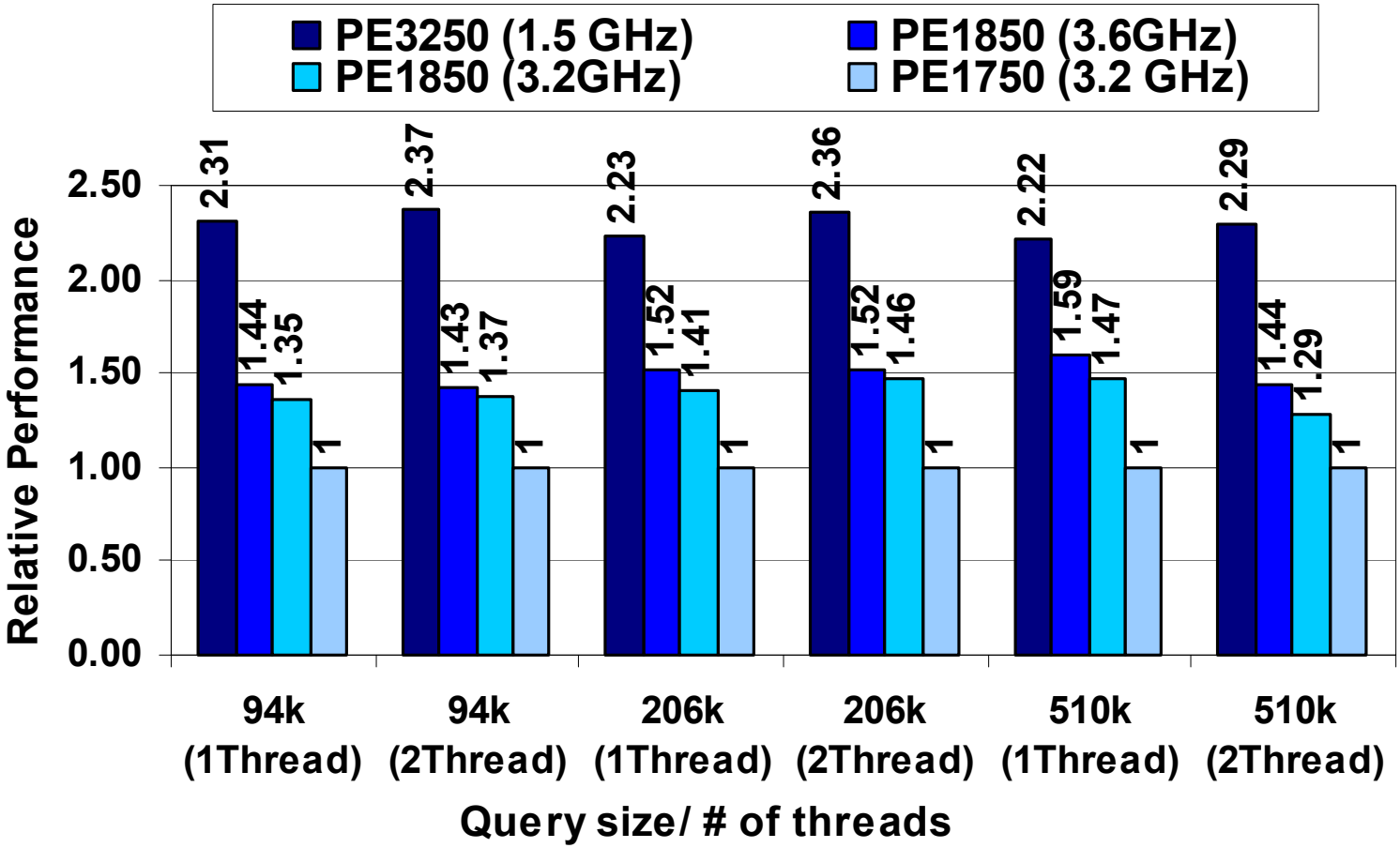
Cache/ Memory Levels	PE1750 3.2 GHz (130nm Xeon) DDR266	PE1850 3.2 GHz (90nm Xeon) DDR2-400	PE3250 1.5 GHz (Itanium2) DDR-200
Time (nano seconds)			
L1	0.63ns	1.25ns	1.34ns
L2	5.7ns	9.03ns	4.02ns
L3	8.5ns	-N/A-	13.7ns
Memory	128ns	116ns	201ns
Cycles (processor clocks)			
L1	2	4	2
L2	18	29	6
L3	27	-N/A-	21
Memory	410	371	302

- **Basic Local Alignment Search Tool**
  - A family of sequence database-search algorithms
  - Searches a database for similarities to a short query sequence



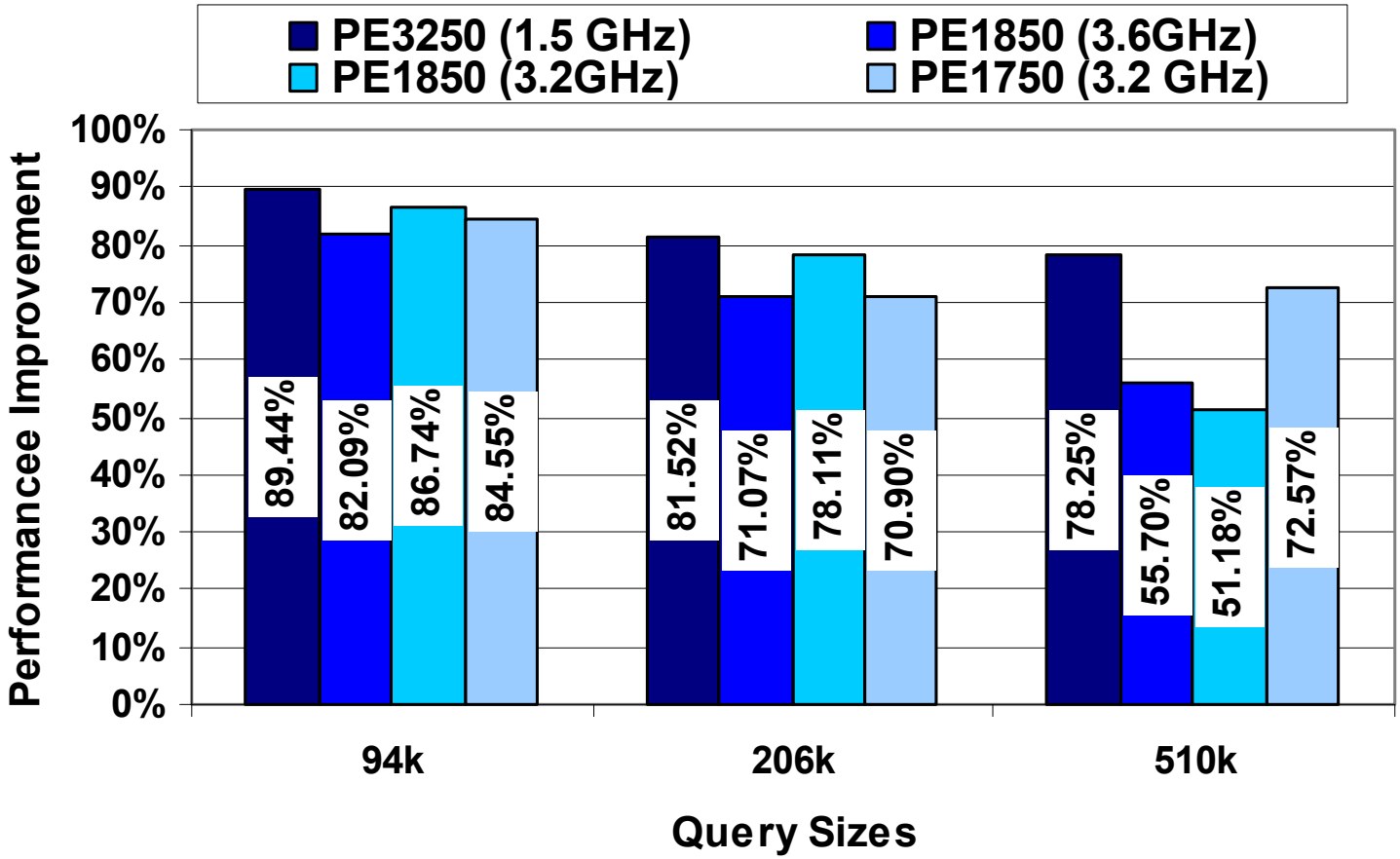
- **Application Characteristics**
  - Sensitive to processor memory bandwidth
  - Embarrassingly parallel operation
  - Integer operation intensive operations

BLAST Performance

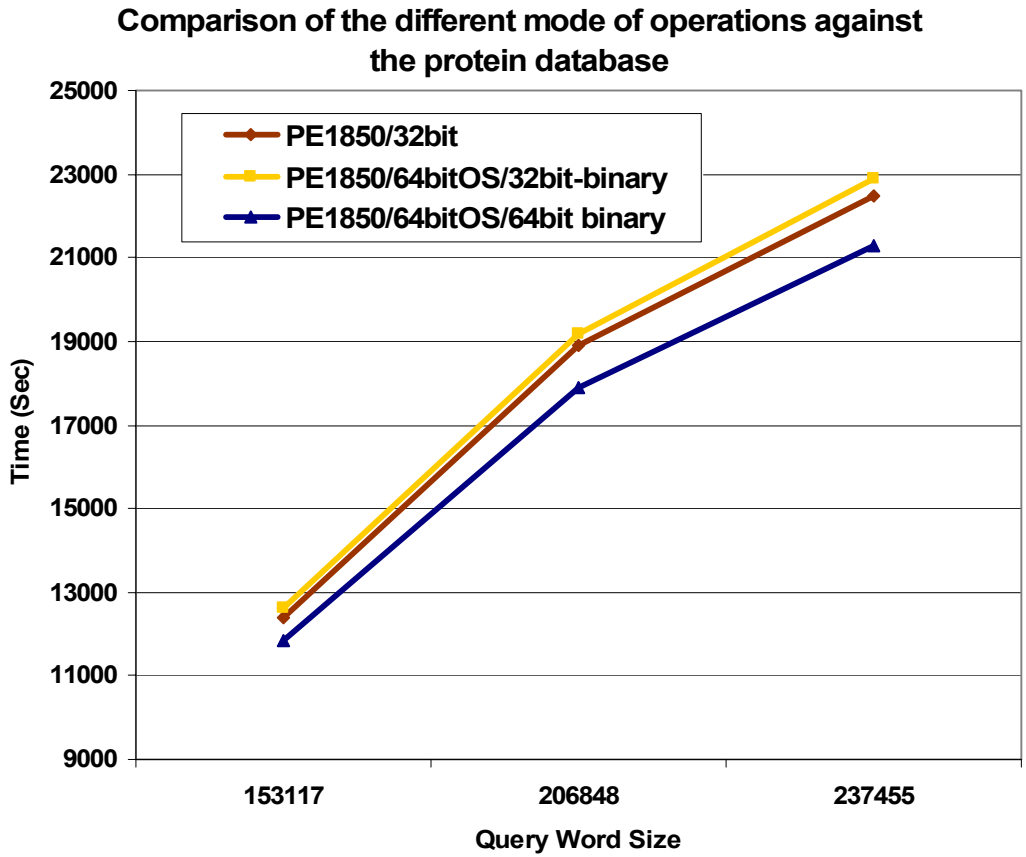


- **PE1850 - 29%-59% performance improvements**
- **PE3250 – 122% - 137% performance improvements**

Scalability (1P to 2P)



- **Good Thread-Level Parallelism**



- **EM64T mode provides benefits with additional registers and memory addressing capability over legacy 32-bit modes.**

CPU Performance Metrics (Xeon)

	PE1750 (3.2GHz)	PE1850 (3.2GHz)	PE1850 (3.6GHz)
% Unhalted CPU Cycles	98.97%	98.53%	98.84%
Path Length	133M	144M	145M
CPI	2.84	2.62	2.93
Instruction Speculation Efficiency Ratio	64%	60%	60%

	PE1750 (3.2GHz)	PE1850 (3.2GHz)	PE1850 (3.6GHz)
L1 Data Cache Miss Ratio	8%	7%	7%
L2 Cache Load & Store Miss Ratio	24%	14%	15%
L2 Cache Hits Shared Ratio	48%	68%	65%
L2 Cache Hits Exclusive Ratio	11%	11%	11%
L2 Cache Hits Modified Ratio	16%	9%	9%
L3 Cache Load & Store Miss Ratio	54%	N/A	N/A

FSB Data Bus Throughput Mbytes/sec	1,132	1,398	1,439

CPU Performance Metrics (Xeon vs. Itanium)

	PE1750 (3.2GHz Xeon)	PE1850 (3.2GHz Xeon)	PE1850 (3.6GHz Xeon)	PE3250 (1.5GHz Itanium2)
CPI	2.84	2.62	2.93	0.68
L1 data Cache miss ratio	8%	7%	7%	15.8%
L2 Cache Miss Ratio	24%	14%	15%	22.3%
L3 Cache Miss Ratio	54%	100%	100%	7.1%

Summary and Future Directions

- **Evaluated Performance of BLAST on different Platforms**
  - **BLAST runs well on IA64 architecture**
  - **Scaled well with faster DDR2 memory**
  - **No large benefits from increased cache size on Nocona**
  - **No additional benefits from 64-bit capabilities**
  - **Interesting workload**

- **Future Work**
  - **Run on a cluster to evaluate**
    - **Interconnect performance**
    - **Different flavors of MPI libraries**
    - **Impact of Hyper-Threading**